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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,355	10/01/2003	Chih-Wei Chen	0698-0164P	3816

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EXAMINER	
PEERS, CHASE W	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,355	CHEN, CHIH-WEI	
	Examiner	Art Unit	
	Chase Peers	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/1/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto (Pat Pub No 20050097540) in further view of Aguilar et al. (Pat No 6892297).

Regarding claim 1: Matsumoto describes a plurality of memory blocks for storing operating info (paragraph 5), an information register for storing update information (paragraph 9), an information register divided into a plurality of update info blocks (also paragraph 9), an addressing module for storing information addresses (paragraphs 51 to 57 and figures 4 to 6), and an information updating module (paragraph 9).

However, Matsumoto does not describe a check sum module or comparing the check sums of the old and updated information. Aguilar et al. does disclose these features in paragraphs 14 and 15

These references are analogous art because they are both regarding updating flash memory. It would have been obvious to one of ordinary skill in the art to combine updating a flash rom with the ability to do a check sum on the new and older modules. Motivation for these combinations would have been increased security and integrity.

Regarding claim 2: Matsumoto and Aguilar et al. describes all of claim 1 and Matsumoto goes on to further describe that the primary information unit is an EPROM (paragraph 68).

Regarding claim 5: Matsumoto and Aguilar et al. describes all of claim 1 and Aguilar et al. goes on further to disclose that the check code is retrieved by performing a check sum on the attributes of each memory block and update information block (paragraphs 14 and 15).

These references are analogous art because they are both regarding updating flash memory. It would have been obvious to one of ordinary skill in the art to combine updating a flash rom with the ability to do a check sum on the new and older modules. Motivation for these combinations would have been increased security and integrity.

Regarding claim 7: Matsumoto and Aguilar et al. describes all of claim 1 and Matsumoto goes on to further teach having the addressing module as a register (paragraph 55 and figures 4-6).

3. Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto and Aguilar et al. as applied to claim 1 above, and further in view of Venkiteswaran (Pat Pub No 20030229752).

Regarding claim 3: Matsumoto and Aguilar et al. describes all of claim 1 above, but do not exclusively disclose having the core operating info include data for BIOS settings or embedded software. However, Venkiteswaran does describe this (paragraph 18).

These references are analogous art because they are both regarding updating flash memory. It would have been obvious to one of ordinary skill in the art to make the core operating info include data for a BIOS or embedded software. Motivation for these combinations would have been the ability to use the claimed invention on a majority of current and future hardware.

4. Claim 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto and Aguilar et al. as applied to claim 1 above, and further in view of Morrison et al. (Pat Pub No 20030106051).

Regarding claim 4: Matsumoto and Aguilar et al. describe all of claim 1 above, but do not disclose having the update information disappear when the power is turned off or having the information be in SRAM or DRAM, this functionality is described by Morrison et al. (paragraph 58).

These references are analogous art because they are both regarding updating flash memory. It would have been obvious to one of ordinary skill in the art to put the update information into volatile RAM. Motivation for these combinations would have been to make sure that the update is removed from the system when the updating process is finished.

5. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto and Aguilar et al. as applied to claim 1 above, and further in view of Dye (Pat No 6145069).

Regarding claim 6: Matsumoto and Aguilar et al. describe all of claim 1 above, but do not expressly disclose having the logic comparison module located in the CPU. Dye does teach having the logic comparison module located in the CPU (paragraph 4).

These references are analogous art because they are both regarding updating flash memory. It would have been obvious to one of ordinary skill in the art to put the logic comparison module in the CPU. Motivation for these combinations would have been to reuse the logic already incorporated in the CPU to save space and money.

6. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto and Aguilar et al. as applied to claim 1 above, and further in view of Bealkowski et al. (Pat No 5878256).

Regarding claim 8: Matsumoto and Aguilar et al. describe all of claim 1, but do not expressly disclose having the information updating module be a ROM burner or burner simulator software, which is taught by Bealkowski et al. (paragraph 73).

These references are analogous art because they are both regarding updating flash memory. It would have been obvious to one of ordinary skill in the art to make the updating module a ROM burner. Motivation for these combinations would have been to

use current methods of installing BIOS updates so that the claimed invention can be more easily used with current hardware and flashing methods.

7. Claims 9-11, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto (Pat Pub No 20050097540) in further view of Aguilar et al. (Pat No 6892297) and Malecek et al. (Pat No 5295255).

Regarding claim 9: Matsumoto teaches having a plurality of memory blocks with primary core information in a memory chip (paragraph 5), inputting updated information via a user (paragraph 254), determining if there's an update command provided with information (paragraph 74), dividing updated information into blocks (paragraph 9), erasing information stored in memory blocks (paragraph 9), writing the information from the update block to the information erased memory block (paragraph 9), and ending the update process (figure 3).

Matsumoto does not disclose performing a check sum on both sets of code and using this check sum to store information addresses associated with inconsistent check codes. Aguilar et al. does teach the use of a check sum (paragraphs 14 and 15).

These references are analogous art because they are both regarding updating flash memory. It would have been obvious to one of ordinary skill in the art to combine updating a flash rom with the ability to do a check sum on the new and older modules. Motivation for these combinations would have been increased security and integrity.

Neither Matsumoto nor Aguilar et al. expressly teaches the use of storing bad addresses, but Malecek et al. does (paragraphs 30, 32, 33 and figure 6).

These references are analogous art because they are both regarding updating flash memory. It would have been obvious to one of ordinary skill in the art to combine updating a flash rom with the ability to do a check sum on the new and older modules and storing the bad addresses. Motivation for these combinations would have been increased security, integrity, and easily erasing the old data and copying the update information.

Regarding claim 10: Matsumoto, Aguilar et al. and Malecek et al. describe all of claim 9. Matsumoto further describes a plurality of memory blocks for storing operating info (paragraph 5), an information register for storing update information (paragraph 9), an information register divided into a plurality of update info blocks (also paragraph 9), an addressing module for storing information addresses (paragraphs 51 to 57 and figures 4 to 6), and an information updating module (paragraph 9).

However, Matsumoto does not describe a check sum module or comparing the check sums of the old and updated information. Aguilar et al. does disclose these features in paragraphs 14 and 15.

These references are analogous art because they are both regarding updating flash memory. It would have been obvious to one of ordinary skill in the art to combine updating a flash rom with the ability to do a check sum on the new and older modules. Motivation for these combinations would have been increased security and integrity.

Regarding claim 11: Matsumoto, Aguilar et al. and Malecek et al. describe all of claim 9 and Aguilar et al. goes on to disclose having the electronic device be a pda, pc, or laptop (paragraph 8 and figure 1). Although Aguilar et al. does not teach the use of a

digital camera or electronic dictionary, it would have been obvious to a person of ordinary skill in the art to incorporate these devices as well. The reasoning behind this would be that these devices would also benefit from the use of this technology since they also have a bios or other embedded software.

Regarding claim 13: Matsumoto, Aguilar et al. and Malecek et al. describe all of claim 9 and Aguilar et al. goes on further to disclose that the check code is retrieved by performing a check sum on the attributes of each memory block and update information block (paragraphs 14 and 15).

These references are analogous art because they are both regarding updating flash memory. It would have been obvious to one of ordinary skill in the art to combine updating a flash rom with the ability to do a check sum on the new and older modules. Motivation for these combinations would have been increased security and integrity.

Regarding claim 14: Matsumoto, Aguilar et al. and Malecek et al. describe all of claims 9 and 10 and Matsumoto goes on to further teach having the addressing module as a register (paragraph 55 and figures 4-6).

8. Claim 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto, Aguilar et al. and Malecek et al. as applied to claim 9 above, and further in view of Venkiteswaran (Pat Pub No 20030229752).

Regarding claim 12: Matsumoto and Aguilar et al. describes all of claim 9 and Matsumoto goes on to further describe having update information blocks sized corresponding to the memory blocks (paragraph 69). Matsumoto does not expressly

teach having the updated information be for BIOS or embedded software, which is taught by Venkiteswaran (paragraph 18).

These references are analogous art because they are both regarding updating flash memory. It would have been obvious to one of ordinary skill in the art to make the core operating info include data for a BIOS or embedded software. Motivation for these combinations would have been the ability to use the claimed invention on a majority of current and future hardware.

9. Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto, Aguilar et al. and Malecek et al. as applied to claims 9 and 10 above, and further in view of Bealkowski et al. (Pat No 5878256).

Regarding claim 15: Matsumoto and Aguilar et al. describe all of claims 9 and 10, but do not expressly disclose having the information updating module be a ROM burner or burner simulator software, which is taught by Bealkowski et al. (paragraph 73).

These references are analogous art because they are both regarding updating flash memory. It would have been obvious to one of ordinary skill in the art to make the updating module a ROM burner. Motivation for these combinations would have been to use current methods of installing BIOS updates so that the claimed invention can be more easily used with current hardware and flashing methods.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chase Peers whose telephone number is (571) 272-

6757. The examiner can normally be reached on from Monday to Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PIERRE BATAILLE
PRIMARY EXAMINER
10/06/05